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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,450	03/31/2004	Anthony L. Chun	1020.P18417	9246

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EXAMINER	
GEIB, BENJAMIN P	

ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/816,450	CHUN ET AL.	
	Examiner	Art Unit	
	Benjamin P. Geib	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004 and 25 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 17-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 17-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-11 and 17-30 have been examined.

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Application on 03/31/2004, Power of Attorney on 06/23/2006, and Response to Restriction on 07/25/2007.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1 and 3-6 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 5, 7, and 8 of copending Application No. 10/816451 ('451). Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1, 5, 7, and 8

of '451 anticipate (i.e. contain every element of) claims 1, 3 & 4, 5, and 6, respectively, of the instant application. Further, claims 9 and 13 of '451 anticipate (i.e. contain every element of) claims 1 and 3 & 4, respectively, of the instant application. This is a provisional obviousness-type double patenting rejection.

5. Claims 2 and 7-11 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1, 5, 7, and 8 of copending Application No. 10/816451 ('451) in view of Fette et al., U.S. Patent No. 4,862,407 (Hereinafter Fette). One of ordinary skill in the art would have been motivated to combine '451 with Fette to fill in the details of the microcode execution system left silent by '451. Citations from Fette for the claim limitations are given below:

Referring to claim 2, Fette has taught wherein execution units comprise a logic unit to perform scalar arithmetic operations, and at least one data path execution unit to perform arithmetic operations *[column 5, line 63 – column 6, line 7]*;

Referring to claim 7, Fette has a data selector to read said input data from a memory unit, and distribute said input data to said execution units *[column 6, lines 14-31]*;

Referring to claim 8, Fette has taught a register file module to store previously read input data during function execution when multiple read cycles are needed to provide data for said function *[data registers (components 30 and 31); column 6, lines 37-41]*;

Referring to claim 9, Fette has taught a data packer to receive processed input data from the execution units, and to send said processed input data to an output buffer *[column 6, lines 14-31]*;

Referring to claim 10, Fette has taught a data router adapter to communicate packets with said routing elements, said data router adapter to distribute data from received packets to a configuration memory or said memory unit, and transmit packets of processed data from said execution units stored in an output buffer *[data bus mux (component 39); column 6, lines 14-31]*;

Referring to claim 11, Fette has taught wherein the logic unit comprises a data address generator to control writing said input data to said memory unit, and reading said input data from said memory unit *[component 32; column 7, lines 3-14]*.

This is a provisional obviousness-type double patenting rejection.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 2, and 7-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Fette et al., U.S. Patent No. 4,862,407 (Hereinafter Fette).

8. Referring to claim 1, Fette has taught an apparatus, comprising:

a memory unit *[dual port memory, FIG. 1, component 19]* to store input data for a plurality of functions *[column 4, line 64 – column 5, line 2]*;

a control unit *[microsequencer; FIG. 2, component 27]* to control execution of said plurality of functions *[column 5, lines 63-65]*, said control unit to select a function to execute using a function identifier *[column 7, lines 15-22]*; and

a plurality of execution units operatively responsive to said control unit, said execution units to receive input data from said memory unit, and use said input data to execute a function corresponding to said function identifier *[column 5, line 63 – column 6, line 7]*.

9. Referring to claim 2, Fette has taught the apparatus of claim 1, wherein said execution units comprise a logic unit to perform scalar arithmetic operations, and at least one data path execution unit to perform arithmetic operations *[column 5, line 63 – column 6, line 7]*.

10. Referring to claim 7, Fette has taught the apparatus of claim 1, further comprising a data selector to read said input data from said memory unit, and distribute said input data to said execution units *[column 6, lines 14-31]*.

11. Referring to claim 8, Fette has taught the apparatus of claim 1, further comprising a register file module to store previously read input data during function execution when multiple read cycles are needed to provide data for said function *[data registers (components 30 and 31); column 6, lines 37-41]*.

12. Referring to claim 9, Fette has taught the apparatus of claim 1, further comprising a data packer to receive processed input data from said execution units, and to send said processed input data to an output buffer *[column 6, lines 14-31].*

13. Referring to claim 10, Fette has taught the apparatus of claim 1, further comprising a data router adapter to communicate packets with said routing elements, said data router adapter to distribute data from received packets to a configuration memory or said memory unit, and transmit packets of processed data from said execution units stored in an output buffer *[data bus mux (component 39); column 6, lines 14-31].*

14. Referring to claim 11, Fette has taught the apparatus of claim 1, wherein said logic unit comprises a data address generator to control writing said input data to said memory unit, and reading said input data from said memory unit *[component 32; column 7, lines 3-14].*

15. Claims 17, 18, 22, 24, 25, and 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Bell et al., U.S. Patent No. 6,081,888 (Hereinafter Bell).

16. Referring to claims 17 and 24, taking claim 24 as exemplary, Bell has taught an article comprising:

a storage medium; said storage medium including stored instructions *[The arithmetic logic unit receives instructions (column 2, lines 35-38), which inherently must be stored in a storage medium]* that, when executed by a processor *[column 2, lines 40-47]*, result in receiving configuration information, configuring a control unit using said

configuration information *[The microcode control store 240 (i.e. control unit) is configured using configuration, or control, information received from the reload control logic; column 3, lines 18-22]*, receiving input data for a plurality of functions, controlling execution of said plurality of functions using control signals, and executing said plurality of functions by a plurality of execution units using said input data in accordance with said control signals *[column 2, lines 24-34]*.

17. Referring to claims 18 and 25, taking claim 25 as exemplary, Bell has taught the article of claim 24, wherein the stored instructions, when executed by a processor, further result in said plurality of functions being executed during different time periods *[column 2, lines 24-34]*.

18. Referring to claims 22 and 29, taking claim 29 as exemplary, Bell has taught the article of claim 24, wherein the stored instructions, when executed by a processor, further result in said executing by receiving said input data at said execution units, receiving function control signals from said control unit, and processing said received input data in accordance with said function control signals *[column 2, lines 24-34]*.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 3-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fette in view of Crabill, U.S. Patent No. 6,725,364.

21. Referring to claim 3, Fette has taught the apparatus of claim 1.

Fette has not explicitly taught that the apparatus further comprises a configuration memory to store configuration parameters for said control unit, said configuration parameters including a fuse map and table content data.

Crabill has taught using configuration parameters to reprogram field programmable gate array microcode storage *[Crabill; column 3, lines 46-50]*. The configuration parameters inherently are from a configuration memory that stores them since the parameter must be stored somewhere. Further, since the microcode storage is programmable gate array storage, the configuration parameters inherently include a fuse map and table content data.

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify the apparatus of Fette to further comprise a configuration memory to store configuration parameters for said control unit, said configuration parameters including a fuse map and table content data as taught by Crabill.

The motivation for doing so would have been that the apparatus would be more flexible *[Crabill; column 1, lines 60-66]*.

22. Referring to claim 4, Fette and Crabill have taught the apparatus of claim 3, wherein said control unit comprises:

a control unit state machine module to be configured in accordance with said fuse map, said control unit state machine to output an operation number address *[Fette; column 8, lines 8-29]*; and

a control unit lookup table to be configured with said table content data, said control unit lookup table to convert said operation number address to a reconfigurator vector, said reconfigurator vector to control execution of said function by said execution units *[Fette; column 8, lines 8-29]*.

23. Referring to claim 5, Fette and Crabill have taught the apparatus of claim 4, wherein said control unit further comprises:

an inner loop counter to count a number of repetitions of instructions in an inner loop, said inner loop counter to output an inner terminal count signal *[Fette; column 7, lines 31-38]*;

an outer loop counter to count a number of repetitions of instructions in an outer loop, said outer loop counter to output an outer terminal count signal *[Fette; column 7, lines 31-38]*; and

a register file module to store a state for one function while another function is being executed by said execution units *[Fette; function register (component 80); column 8, lines 8-13]*.

24. Referring to claim 6, Fette and Crabill have taught the apparatus of claim 5, wherein said control unit state machine module receives as inputs said inner terminal count signal, said outer terminal count signal, said function identifier, a current state

index value, and status register values from said execution units, and uses said inputs to generate said operation number address *[Fette; column 8, lines 8-29]*.

25. Claims 19 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bell in view of Crabill.

26. Referring to claims 19 and 26, taking claim 26 as exemplary, Bell has taught the article of claim 24, wherein the stored instructions, when executed by a processor, further result in said configuring by receiving configuration parameters for said control unit.

Bell has not explicitly taught that said configuration parameters include a fuse map and table content data, and configuring a control unit state machine module using said fuse map, and configuring a control unit lookup table using said table content data.

Crabill has taught using configuration parameters to reprogram field programmable gate array microcode storage *[Crabill; column 3, lines 46-50]*. Since the microcode storage is programmable gate array storage, the configuration parameters inherently include a fuse map and table content data. In programming the microcode storage a control unit state machine module would be configured using said fuse map, and a control unit lookup table would be configured using said table content data.

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify the article of Bell so that the configuration parameters include a fuse map and table content data, and configuring a control unit state machine

module using said fuse map, and configuring a control unit lookup table using said table content data as taught by Crabill.

The motivation for doing so would have been that the apparatus would be more flexible *[Crabill; column 1, lines 60-66]*.

27. Claims 20, 21, 23, 27, 28, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bell in view of Fette.

28. Referring to claims 20 and 27, taking claim 27 as exemplary, Bell has taught the article of claim 24.

Bell is silent on the details of the microcode control store and, therefore, has not explicitly taught wherein the stored instructions, when executed by a processor, further result in said controlling by reading a function identifier for a function from a function list, generating a reconfigurator vector using said function identifier, sending a data select signal to a data selector to read input data from an input buffer in accordance with said reconfigurator vector, and sending function control signals to said execution units to process said input data in accordance with said reconfigurator vector.

Fette has taught a processor wherein stored instructions, when executed by a processor, further result in said controlling by reading a function identifier for a function from a function list, generating a reconfigurator vector using said function identifier, sending a data select signal to a data selector to read input data from an input buffer in accordance with said reconfigurator vector, and sending function control signals to said

execution units to process input data in accordance with said reconfigurator vector *[Fette; column 5, line 63 – column 6, line 7; column 7, lines 15-22].*

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify the article of Bell so that the stored instructions, when executed by a processor, further result in said controlling by reading a function identifier for a function from a function list, generating a reconfigurator vector using said function identifier, sending a data select signal to a data selector to read input data from an input buffer in accordance with said reconfigurator vector, and sending function control signals to said execution units to process said input data in accordance with said reconfigurator vector as taught by Fette.

The motivation for doing so would have been to fill in the details of the microcode control store.

29. Referring to claims 21 and 28, taking claim 28 as exemplary, Bell and Fette have taught the article of claim 27, wherein the stored instructions, when executed by a processor, further result in said generating by receiving as inputs an inner terminal count signal, an outer terminal count signal, said function identifier, a current state index value, and status register values from said execution units, at said control unit state machine, generating an operation number address using said inputs, converting said operation number address to a reconfigurator vector, said reconfigurator vector to control execution of said function by said execution units *[Fette; column 7, lines 31-38].*

30. Referring to claims 23 and 30, taking claim 30 as exemplary, Bell and Fette have taught the article of claim 24, wherein the stored instructions, when executed by a

processor, further result in said receiving by receiving a function identifier and an input identifier for each function, creating an input buffer corresponding to each input identifier, and writing input data for each function in said corresponding input buffer *[Fette; column 8, lines 8-29].*

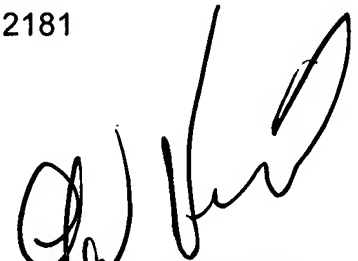
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Benjamin P Geib
Examiner
Art Unit 2181



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